Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1. (Canceled)

Claim 2. (Currently Amended) The method of claim ~~21~~22, wherein the set of boundary scan registers include a plurality of shift registers connected in series, wherein each shift register is adapted to be connected with an interface connection of the IP core.

Claim 3. (Original) The method of claim 2, wherein a first portion of the plurality of shift registers is adapted to be connected with a set of input interface connections of the IP core and a second portion of the plurality of shift registers is adapted to be connected with a set of output interface connections of the IP core.

Claim 4. (Currently Amended) The method of claim ~~21~~22, wherein the test configuration is defined with a hardware description language representation.

Claim 5. (Original) The method of claim 4, wherein the creating a test program includes:

combining the hardware description language representation of the test configuration with a hardware description language representation of the IP core to form a test hardware description; and

analyzing the test hardware description to create a set of test data.

Claim 6. (Original) The method of claim 5, wherein creating a test program further includes analyzing the test hardware description and the set of test data to create a set of expected test results; and

wherein analyzing the test results includes comparing the set of test results with the set of expected test results.

Claim 7. (Original) The method of claim 5, wherein analyzing the test hardware description is performed using automated test program generation software.

Claim 8. (Canceled)

Claim 9. (Previously Presented) The information storage medium of claim 24, wherein the set of boundary scan registers include a plurality of shift registers connected in series, wherein each shift register is adapted to be connected with an interface connection of the IP core.

Claim 10. (Original) The information storage medium of claim 9, wherein a first portion of the plurality of shift registers is adapted to be connected with a set of input interface connections of the IP core and a second portion of the plurality of shift registers is adapted to be connected with a set of output interface connections of the IP core.

Claim 11. (Previously Presented) The information storage medium of claim 24, wherein the test configuration is defined with a hardware description language representation.

Claim 12. (Original) The information storage medium of claim 11, wherein the creating a test program includes:

combining the hardware description language representation of the test configuration with a hardware description language representation of the IP core to form a test hardware description; and

analyzing the test hardware description to create a set of test data.

Claim 13. (Previously Presented) The information storage medium of claim 12, wherein creating a test program further includes analyzing the test hardware description and the set of test data to create a set of expected test results; and

wherein analyzing the set of test results includes comparing the set of test results with the set of expected test results.

Claim 14. (Original) The information storage medium of claim 12, wherein analyzing the test hardware description is performed using automated test program generation software.

Claim 15. (Canceled)

Claim 16. (Currently Amended) The reconfigurable device of claim ~~25~~26, wherein the set of boundary scan registers include a plurality of shift registers connected in series, wherein each shift register is adapted to be connected with an interface connection of the IP core.

Claim 17. (Previously Presented) The reconfigurable device of claim 16, wherein a first portion of the plurality of shift registers is adapted to be connected with a set of input interface connections of the IP core and a second portion of the plurality of shift registers is adapted to be connected with a set of output interface connections of the IP core.

Claim 18. (Currently Amended) The reconfigurable device of claim ~~25~~26, wherein the test configuration is defined with a hardware description language representation.

Claim 19. (Currently Amended) The reconfigurable device of claim ~~25~~26, wherein the information storage medium further includes a set of test data adapted to be input into the IP core via the set of functional blocks implementing the set of boundary scan registers.

Claim 20. (Currently Amended) The reconfigurable device of claim ~~25~~26, wherein the information storage medium further includes a set of expected test results.

Claim 21. (Canceled)

Claim 22. (Currently Amended) ~~The method of claim 21~~ A method for testing a set of interface connections in a reconfigurable device between an IP core implementing at least one specialized operation and a set of functional blocks adapted to implement general-purpose logic devices, the method comprising:

creating a test program including a set of test data and a test configuration adapted to configure the set of functional blocks to implement a set of boundary scan registers connected with the interface connections of the IP core;

configuring the reconfigurable device according to the test configuration;

inputting the test data into the reconfigurable device to create a set of test results; and

analyzing the set of test results to determine the integrity of the set of interface connections,

wherein when the reconfigurable device is configured in the test configuration, the set of functional blocks are configured to implement the set of boundary scan registers, the set of boundary scan registers including at least one input register, the input register having an input coupled to an output of a multiplexer and an output coupled to a first input of a logic gate, where a select input for the multiplexer is coupled to a second input of the logic gate and an output of the logic gate is coupled to an input of the IP core, wherein the output of the logic gate provides an output signal to an input of the multiplexer, and wherein the output of the input register provides a signal to an input of another input register in the set of boundary scan registers.

Claim 23. (Canceled)

Claim 24. (Currently Amended) An information storage medium including a set of instructions ~~adapted~~ therein to ~~operate~~ cause an information processing device to perform a set of steps, the set of steps comprising:

creating a test program including a set of test data and a test configuration adapted to configure a set of functional blocks to implement a set of boundary scan registers connected with interface connections of an IP core;

configuring a reconfigurable device according to the test configuration, the reconfigurable device comprising the functional blocks and IP core;

inputting the set of test data into the reconfigurable device to create a set of test results; and

analyzing the set of test results to determine the integrity of the set of interface connections,

wherein when the reconfigurable device is configured in the test configuration, the set of functional blocks are configured to implement the set of boundary scan registers, the set of boundary scan registers including at least one input register, the input register having an input coupled to an output of a multiplexer and an output coupled to a first input of a logic gate, where a select input for the multiplexer is coupled to a second input of the logic gate and an output of the logic gate is coupled to an input of the IP core, wherein the output of the logic gate provides an output signal to an input of the multiplexer, and wherein the output of the input register provides a signal to an input of another input register in the set of boundary scan registers.

Claim 25. (Canceled)

Claim 26. (Currently Amended) ~~The reconfigurable device of claim 25~~A reconfigurable device comprising an information storage medium including a test configuration for configuring the reconfigurable device, the reconfigurable device having an IP core implementing at least one specialized operation and a set of functional blocks adapted to implement general-purpose logic devices, the test configuration comprising a configuration of the set of functional blocks implementing a set of boundary scan registers connected with a set of interface connections of the IP core,

wherein when the reconfigurable device is configured in the test configuration, the set of functional blocks are configured to implement the set of boundary scan registers, the set of boundary scan registers including at least one input register, the input register having an input coupled to an output of a multiplexer and an output coupled to a first input of a logic gate, where a select input for the multiplexer is coupled to a second input of the logic gate and an output of the logic gate is coupled to an input of the IP core,

wherein when the reconfigurable device is configured in the test configuration, the set of functional blocks are configured to implement the set of boundary scan registers, the set of boundary scan registers including at least one input register, the input register having an

input coupled to an output of a multiplexer and an output coupled to a first input of a logic gate, where a select input for the multiplexer is coupled to a second input of the logic gate and an output of the logic gate is coupled to an input of the IP core, wherein the output of the logic gate provides an output signal to an input of the multiplexer, and wherein the output of the input register provides a signal to an input of another input register in the set of boundary scan registers.